Minimax Theory and its Applications

Volume 11 (2026), No. 3s, 509 to 519

FPGA-Optimized Low-Power Content Addressable Memory for Energy-efficient and high-performance Search Systems

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Abstract
Content-Addressable Memory (CAM) is crucial for high-speed search operations and pattern-matching applications such as networking, standard security, and edge computing systems. However, when directly translated onto Field-Programmable Gate Arrays (FPGAs), typical CAM architectures show excessive power consumption and poor resource efficiency because they are primarily intended for ASIC implementations. This study introduces a new power-aware FPGA-optimized Low-Power Content-Addressable Memory (LPCAM) architecture that is especially made for reconfigurable platforms in order to overcome these difficulties. To drastically cut down on needless switching during search operations, the suggested LPCAM makes use of adaptive match-line activation and selective evaluation techniques. The suggested method minimizes dynamic power usage by only activating the necessary match-lines based on the input search pattern, in contrast to conventional CAM systems that evaluate all match-lines simultaneously. Because the architecture avoids ASIC-specific circuit dependencies and is implemented using LUT-based CAM cells with enable-controlled comparison logic, it is ideal for FPGA fabrics. The Vivado design suite is used to implement and validate the LPCAM design on a Xilinx Zynq-7000 (ZC7020) FPGA. Additionally, the proposed architecture shows better scalability and logic consumption, which makes it appropriate for high-performance and power-constrained search applications.

Keywords— FPGA, low power CAM, matchline, search latency, SoC implementation.

Introduction

The need for high-speed search and pattern-matching technologies has grown dramatically due to the quick development of contemporary computing architectures. Conventional memory architectures use memory addresses to obtain data, necessitating several comparison operations during search procedures, which frequently results in increased latency and computational cost. On the other hand, Content Addressable Memory (CAM) allows constant-time lookup performance regardless of memory size by executing parallel search operations by simultaneously comparing an input search key against all stored items. CAM is now widely utilized in applications including data compression, large data analytics, image and video processing, and hardware accelerators due to its remarkable search capabilities [1], [2].

Conventional CAM architectures have substantial power consumption and scalability issues despite their benefits. Every search operation involves the simultaneous activation and evaluation of all match-lines, which results in excessive switching activity and dynamic power consumption. As CAM size increases, the associated parallel comparison circuitry and match-line capacitance both contribute to increased energy consumption and decreased efficiency [3]. Precomputation-based CAMs [7], segmented match-line architectures [19], shared match-line schemes [6], selective precharge methods [15], and precharge-free CAM designs [10], [11] are only a few of the low-power CAM techniques that have been suggested in the literature. By minimizing needless match-line transitions and improving sensing processes, these methods have shown significant increases in power efficiency.

To further increase energy efficiency, recent research has concentrated on sophisticated match-line control and sensing techniques. While Taco et al. [14], [15] suggested reliable precharge-free CAM architectures that enhance both performance and energy efficiency, Hussain et al. [18] developed a two-layer P-N match-line control architecture to lower power dissipation. In a similar vein, hierarchical search techniques are used by

SMS-CAM [6] and segmented CAM designs [19] to minimize pointless comparisons and match-line activity. The majority of these solutions aim at ASIC implementations and are created utilizing transistor-level CMOS design methodologies, despite the fact that they offer significant benefits. Because of variations in architectural resources, routing architectures, and logic realization techniques, their direct implementation on Field-Programmable Gate Arrays (FPGAs) is frequently inefficient.

FPGAs' versatility, low development costs, and quick prototyping capabilities have made them appealing platforms for creating reconfigurable and application-specific accelerators [34]. High-performance search engines and data processing systems can be implemented using modern FPGA devices because they offer a large number of programmable interconnects, embedded memory, and adjustable logic blocks. However, conventional CAM designs are not inherently compatible with FPGA fabrics. Reduced operating frequency, increased power consumption, improper routing, and excessive LUT utilization are common outcomes of directly mapping ASIC-oriented CAM structures onto FPGAs. Therefore, low power consumption and development continue to be major research challenges.

to circumvent (LPCAM) architecture that employs Adaptive Match-Line Activation (AMLA) and Selective Match-Line Evaluation (SMLE) techniques. The suggested architecture only selectively activates the potential match-lines connected to the incoming search pattern, in contrast to conventional CAMs that activate all match-lines during each search operation. As a result, switching activity, dynamic power consumption, and unnecessary comparison operations are all significantly reduced. The architecture also uses enable-controlled comparison logic in LUT-based CAM cells, which ensures high search throughput and efficient use of FPGA resources. The recommended design is implemented and verified on a Xilinx Zynq-7000 (ZC7020) FPGA using the Vivado Design Suite.

The primary contributions of this research are summarized as follows:

1) Development of FPGA-oriented LPCAM architecture that reduces needless match-line switching by utilizing Adaptive Match-Line Activation (AMLA).
2) In order to reduce dynamic power usage, a Selective Match-Line Evaluation (SMLE) method is introduced that only compares rows that are enabled.
3) LUT-based FPGA-compatible CAM cells with great search performance that do not require ASIC-specific precharge and sensing circuitry.
4) thorough analysis showing gains in FPGA resource use, power consumption, and search performance over traditional CAM and current LPCAM systems.

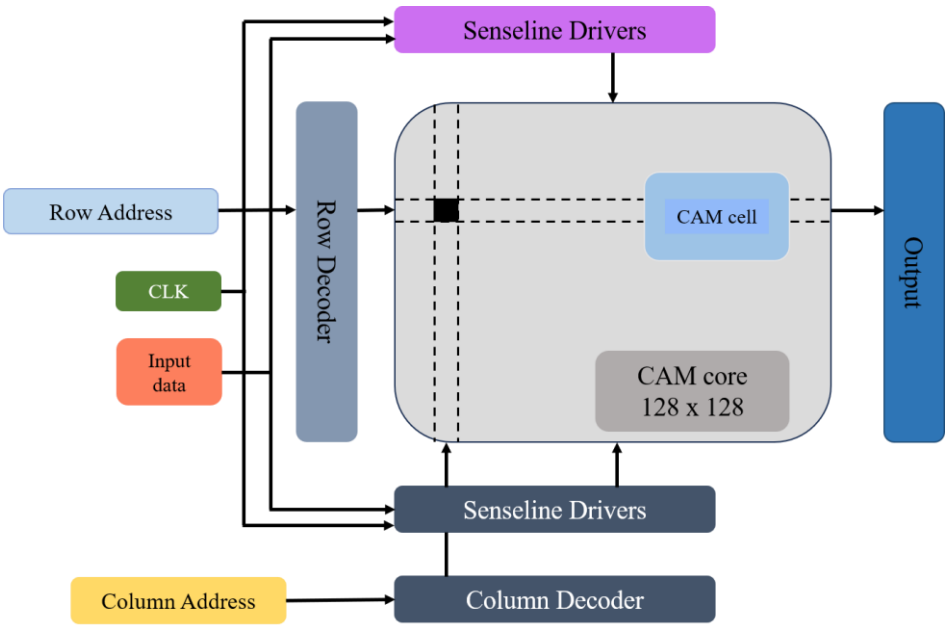


Figure 1. Basic CAM architecture.

The paper is organized as follows. Section II analyses the existing CAM architectures and their limitations. Section III explains the proposed FPGA based low-power CAM (LPCAM) architecture and Section IV discusses the simulation results with concluding highlights in section V.

Related Works

For high-speed search applications like packet categorization, IP routing, database indexing, intrusion detection, and pattern matching, Content Addressable Memory (CAM) has emerged as a crucial hardware component. In contrast to traditional memory systems, CAM allows constant-time search operations by performing concurrent comparison operations across all stored items. However, because match-lines and search circuitry are activated simultaneously, this parallelism leads to high power consumption.

Pagiamtzis and Sheikholeslami [1] conducted one of the first thorough studies on CAM architectures, surveying several CAM organizations, sensing methods, and power-reduction strategies. Subsequently, Karam et al. [2] explored the function of CAM in developing high-performance computing systems and emphasized its growing significance in memory-centric computing.Reducing power dissipation through match-line optimization has been a prominent area of research. When compared to traditional NOR-CAM designs, Chaudhary and Clark's [3] low-power NAND match-line architecture dramatically decreased switching activity. A master-slave match-line design that reduced needless match-line transitions during search operations was presented by Chang and Wu [4]. [6] developed SMS-CAM, which included a shared match-line technique that reduced energy consumption by enabling neighboring CAM cells to share evaluation routes, in order to further reduce power consumption. Precomputation-based search strategies have been studied by a number of researchers to get rid of pointless comparisons. A low-power precomputation-based CAM architecture that completes partial comparisons prior to full search activation was presented by Lin et al. [7]. This idea was further developed by Ruan et al. [8], who created a low-power precomputation method that can lower dynamic switching activity. Later, Pai et al. [9] proposed an enhanced comparison circuit for precomputation-based CAMs that maintained search performance while achieving greater power efficiency.

Another important area of CAM study is precharge optimization. A precharge-free CAM design that does away with traditional match-line precharging procedures was proposed by Zackriya and Kittur [10]. Later, Mahendra et al. [11] enhanced this idea by using a self-controlled precharge-free CAM architecture that decreased search energy and latency. A low-discharge precharge-free match-line construction for energy-efficient search operations was subsequently presented by Mahendra et al. [12]. To further minimize dynamic power loss, Choi et al. [13] suggested a selective match-line precharge system based on charge-sharing strategies. The development of precharge-free designs has continued in recent studies. An energy-efficient precharge-free CAM architecture was presented by Taco et al. [14], which dramatically decreased search energy while preserving reliable performance under process changes. In a further study, Taco et al. [15] presented a precharge-free CAM design based on static transmission gates that can achieve search speeds comparable to high-performance NOR-CAMs while consuming significantly less energy.

Wang et al. [16] suggested a self-disabled sensing technique that halts sensing activities when a mismatch is exposed. Mishra et al. conducted a comprehensive analysis of several sensing techniques and their impact on power and performance [17]. Hussain et al. [18] introduced a two-layer P-N match-line sensing system that improved search reliability and energy economy. Segmentation and hierarchical search methods have been thoroughly studied for power reduction. Ng and Hsu [19] introduced a parallel-segmented CAM architecture that splits search operations into many segments. Ahn and Kwon [20] developed a local NOR and global NAND architecture that reduces switching activity and improves performance. To improve speed and power economy, Ali and Islam [21] suggested a match-line segmentation method with feedback-assisted sensing. Numerous adaptive power-management techniques have also been investigated by researchers. A low-power CAM architecture that offers an effective power-delay trade-off was presented by Do et al. [22]. A parity-assisted CAM architecture with power-gated match-line sensing was later proposed by Do et al. [23]. An early prediction and precharge termination approach that reduces needless match-line activity was further developed by Zackriya and Kittur [24]. In order to lower dynamic power consumption, voltage swing optimization approaches have also been studied. A self-adjustable match-line voltage swing system that can save search energy while maintaining dependable operation was proposed by Mathan and Ravichandran [25]. There have also been reports of high-performance, pipeline-based CAM architectures. A pipelined CAM architecture that increases throughput while preserving low power consumption was proposed by Jiang et al. [26]. A 200 MHz pipeline CAM with incredibly low search energy was demonstrated by Fary et al. [27] using 28 nm CMOS technology. A fast 128 × 128-bit CAM architecture designed for large parallel searches was introduced by Agarwal et al. [28].

Researchers have investigated new memory technologies in addition to CMOS-based CAM implementations. An MTJ-based non-volatile TCAM cell was proposed by Song et al. [29] for dependable search operations. In order to address low-power and high-reliability applications, Wang et al. [30], [31] created a number of non-volatile TCAM architectures based on magnetic tunnel junctions (MTJ). Variation-tolerant non-volatile TCAM designs were further studied by Cho et al. [32]. For low-power associative computing, Deng et al. [33] suggested multi-

context CAM systems using magnetic tunnel junctions. Precharge circuits, charge-sharing networks, custom sensing amplifiers, voltage swing control mechanisms, shared match-lines, and specialized transistor structures are examples of ASIC-specific transistor-level optimizations that are heavily relied upon by most current CAM architectures despite these notable advancements. It is challenging to effectively map such methods onto FPGA fabrics, where routing resources and customizable LUTs are used to implement logic. Therefore, FPGA-oriented CAM architectures that can lower switching activity without necessitating transistor-level changes are still needed.

Proposed FPGA-based LPCAM

The proposed FPGA-Based Low-Power Content Addressable Memory (LPCAM) architecture aims to solve the high-power consumption and resource inefficiencies of conventional CAM implementations on Field Programmable Gate Arrays (FPGAs). Because they engage all match-lines simultaneously during each search operation, conventional CAM systems have limited scalability, excessive switching activity, and increased dynamic power consumption. The earlier LPCAM architecture was not optimized for FPGA fabrics, even if low-power match-line sensing technologies were used to lower power consumption. To get over these limitations, this work provides an FPGA-oriented LPCAM architecture that combines Adaptive Match-Line Activation (AMLA) and Selective Match-Line Evaluation (SMLE) approaches.

Pattern Analyzer, Row Enable Generator, LUT-Based CAM Array, Match-Line Evaluation Unit, and Priority Encoder are the five main functional components that make up the overall architecture as shown in Figure 2. Together, these modules minimize needless switching activity while executing high-speed search operations. Instead of depending on ASIC-specific circuit architectures, the architecture is specifically made to take advantage of FPGA Look-Up Table (LUT) resources, which improves portability and implementation efficiency on reconfigurable systems.

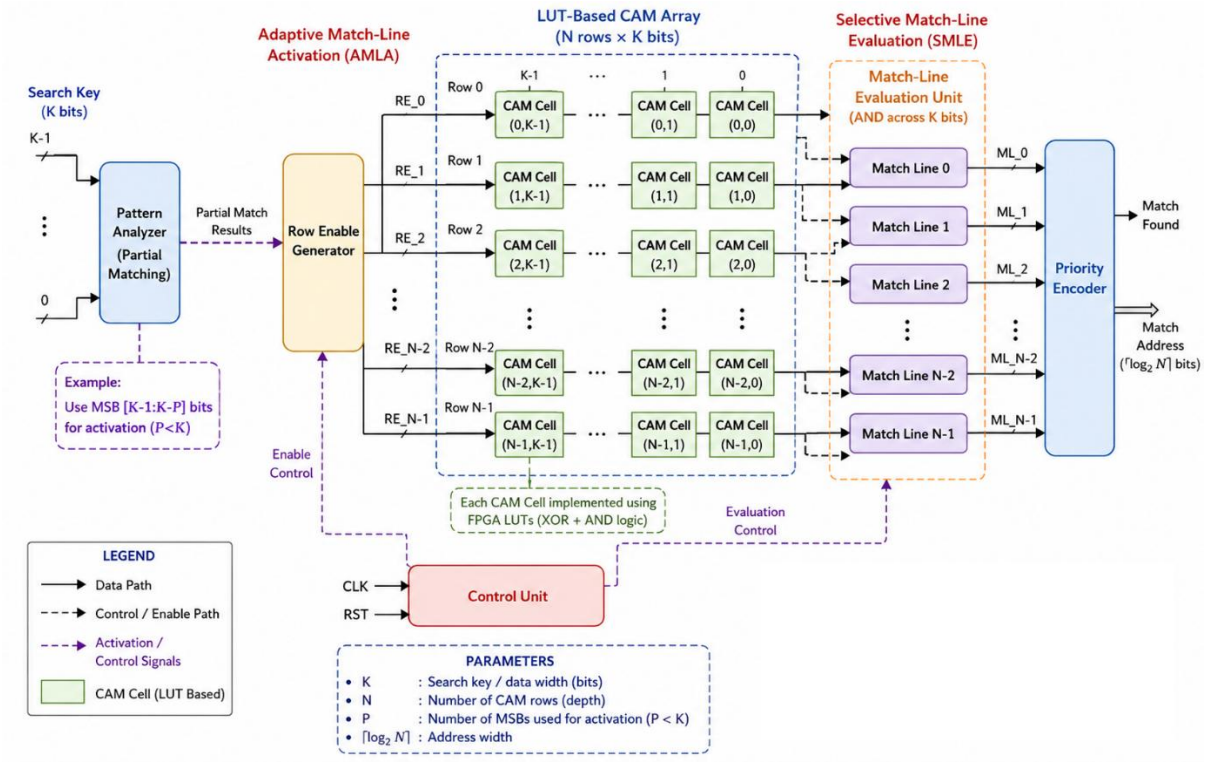


Figure 2. Proposed FPGA based LPCAM architecture.

Pattern Analyzer

The initial step in the search procedure is the Pattern Analyzer. The Pattern Analyzer compares the most important bits of the search pattern with the corresponding bits of all stored entries when a search key is applied. Only rows that meet the preliminary matching requirement are chosen for additional analysis, as opposed to

activating every row in the CAM array. The number of active comparison processes is greatly decreased by this early filtering procedure. For an 8-bit CAM entry, the upper four bits are utilized as activation criteria:row_Enable(i) = 1, if Search_Key[7:4] = CAM_Row(i)[7:4]; Otherwise, row_Enable(i) = 0. This technique minimizes switching transitions throughout the memory array and stops needless activation of unconnected rows.

Row Enable Generator

After receiving the activation data from the Pattern Analyzer, the Row Enable Generator generates enable signals that are distinct to each row. Every enable signal determines whether a specific row takes part in the comparison procedure. Throughout the search cycle, rows that don't meet the activation requirement stay dormant. As a result, power dissipation resulting from redundant evaluations is significantly decreased. By efficiently dividing the CAM array into active and inactive sections, the row enable logic enables the design to concentrate computational resources solely on possibly matching entries.

LUT-Based CAM Array

The suggested architecture's storage and comparison engine is the LUT-Based CAM Array. The suggested solution directly translates CAM functionality onto FPGA LUT resources, in contrast to ASIC-oriented CAM implementations that depend on specialized transistor-level match circuits. Using XOR-based matching logic, each CAM cell compares the stored data and the search key bitwise. The matching row enable signal gates the comparison output. As a result, only when the Pattern Analyzer activates the row does comparison action take place. The bit-level matching operation can be expressed as:

$$Bit_Match = Enable \times \neg(Search_Bit \oplus Stored_Bit) \quad (1)$$

This implementation technique maintains high-speed search performance while making effective use of FPGA logic resources.

Selective Match-Line Evaluation Unit

The main innovation of the suggested architecture is the Selective Match-Line Evaluation Unit. Regardless of the probability of a match, conventional CAM systems assess all match-lines throughout each search operation. Large-scale switching activity caused by this behavior leads to considerable dynamic power usage. The suggested design, on the other hand, only assesses match-lines for rows that the Row Enable Generator has engaged. A logical AND operation is used to each bit-match output of a row to create the match-line for that row. Significant power savings are achieved because idle rows never take part in match-line generation, eliminating needless transitions.

$$Match_Line(i) = Row_Enable(i) \times \prod Bit_Match(i,j) \quad (2)$$

Priority Encoder

The address of the matched entry is ascertained by the Priority Encoder after receiving the match-line outputs from each active row. The encoder uses predetermined addressing rules to choose the highest-priority matching row when there are multiple matches.Two outputs are produced by the encoder: (i) A valid match is indicated by the Match_Found signal and (ii) Match_Address, which indicates where the matched entry is located.

FPGA Optimization Strategy

One of the primary objectives of the proposed architecture is FPGA compatibility. This architecture avoids sensing amplifiers, transistor-level precharge circuits, and ASIC-specific match-line topologies. Rather, it makes use of enable-controlled evaluation units that translate naturally onto FPGA fabrics and LUT-based comparison logic.Selective activation reduces routing congestion, dynamic power usage, and logic toggling. Additionally, without the need for specialized hardware resources, the design may be effectively synthesized using Vivado Design Suite and implemented on Xilinx Zynq-7000 FPGA devices. The implemented design of proposed LPCAM on Zynq SoC is shown in Figure 3.

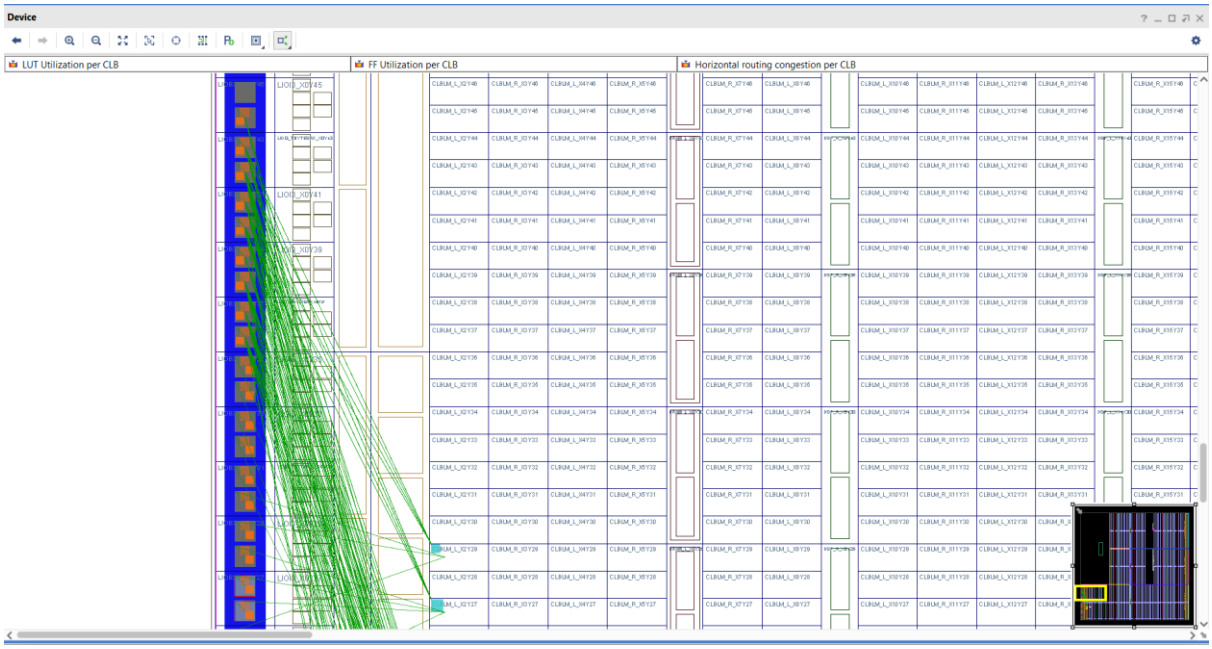


Figure 3. Implemented design of proposed FPGA based LPCAM architecture.

Results and Discussion

AMD Vivado 2020 is used to implement the proposed FPGA-based LPCAM on the Zynq 7000 SoC ZC702.2 on a PC running a 4.4 GHz i5 processor. The schematic representation of proposed FPGA-based LPCAM is shown in Figure 4.

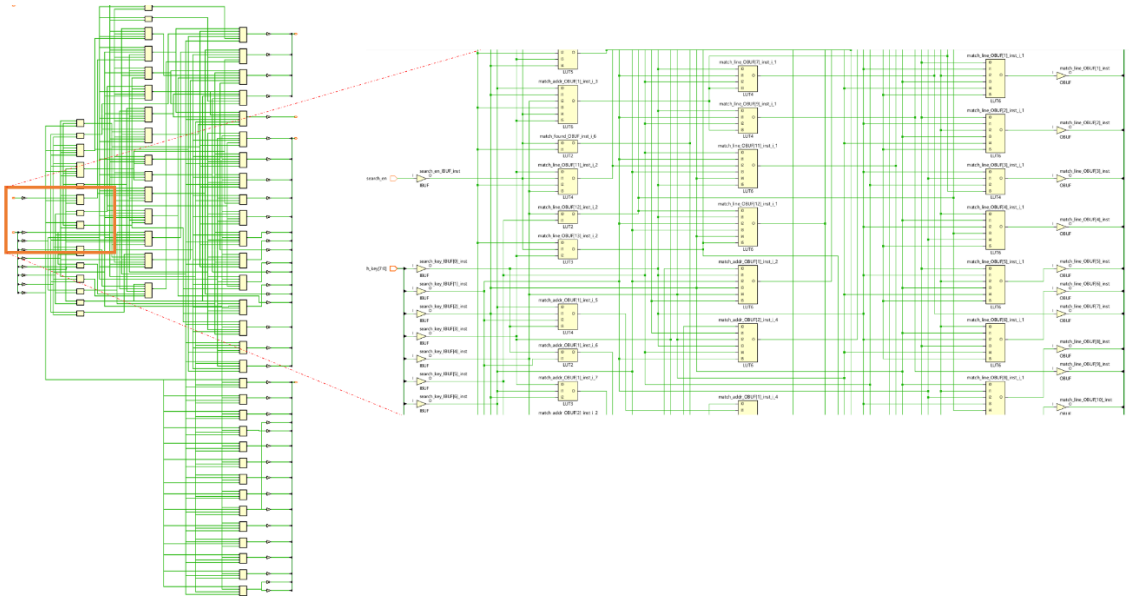
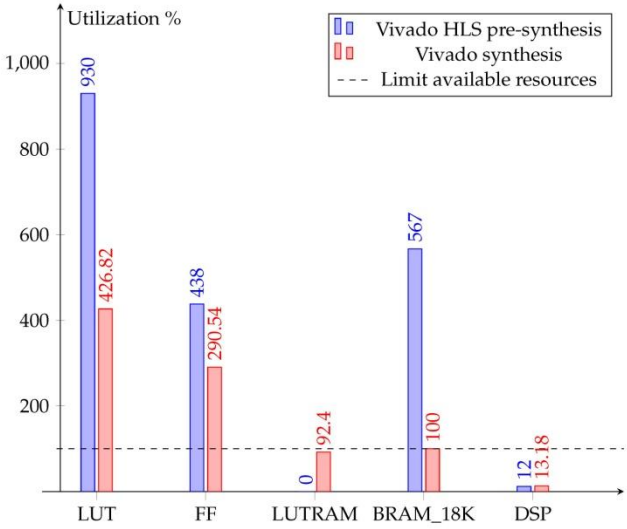


Figure 4. RTL schematic of proposed LPCAM.

The FPGA resource utilization for the proposed FPGA-based LPCAM architecture is shown in Figure 5 based on Vivado synthesis. The findings contrast the actual utilization following synthesis implementation with the resource estimates produced during the HLS pre-synthesis stage. It is evident that Vivado's synthesis optimization greatly lowers hardware resource consumption for all of the main FPGA resources. Logic optimization and resource sharing cause the Look-Up Table (LUT) use to drop significantly, from 930 during pre-synthesis estimation to 426.82 following synthesis. In a similar way, efficient register allocation during synthesis is indicated by a decrease in Flip-Flop (FF) consumption from 438 to 290.54. Additionally, the BRAM utilization shows an impressive decrease from 567 blocks to just 100 blocks during synthesis, demonstrating the efficacy of the memory mapping technique used in the suggested design. With a value of 92.4, LUTRAM

consumption is introduced during synthesis, however this helps to lessen the overall reliance on specialized BRAM resources. With only 13.18 DSP blocks used, DSP usage is still incredibly low, indicating that the suggested architecture mostly depends on FPGA logic resources rather than computationally costly DSP units. Overall, the synthesis results verify that the suggested FPGA-based LPCAM architecture maintains good search speed while effectively utilizing FPGA resources.



Figure

The functional verification waveform of the suggested FPGA-based Low Power Content Addressable Memory (LPCAM) is shown in Figure 5. The waveform illustrates several search circumstances, such as selective evaluation operations, adaptive match-line activation, mismatch, and successful match. The search key value 10101010 is first applied to the CAM array, producing a successful match condition in which the match address is created appropriately and the matching match-line is asserted. When the search key is then changed to 11111111, there is no matching entry in the memory array, resulting in a search miss condition where the match-found signal is removed and all match-lines remain idle. The waveform as shown in Figure 5 also validates the adaptive match-line activation scheme utilized in the proposed design. Not all rows are active at the same time. Only the rows meeting the activation requirements are enabled for comparison. As a result, the row-enable signals selectively activate some CAM rows while leaving the remaining rows inactive. This targeted evaluation reduces the unnecessary switching activity of the FPGA fabric significantly. Moreover, the waveform shows the correct address generation and the match detection capacity under different search scenarios, which verifies the correctness and resilience of the suggested LPCAM architecture.

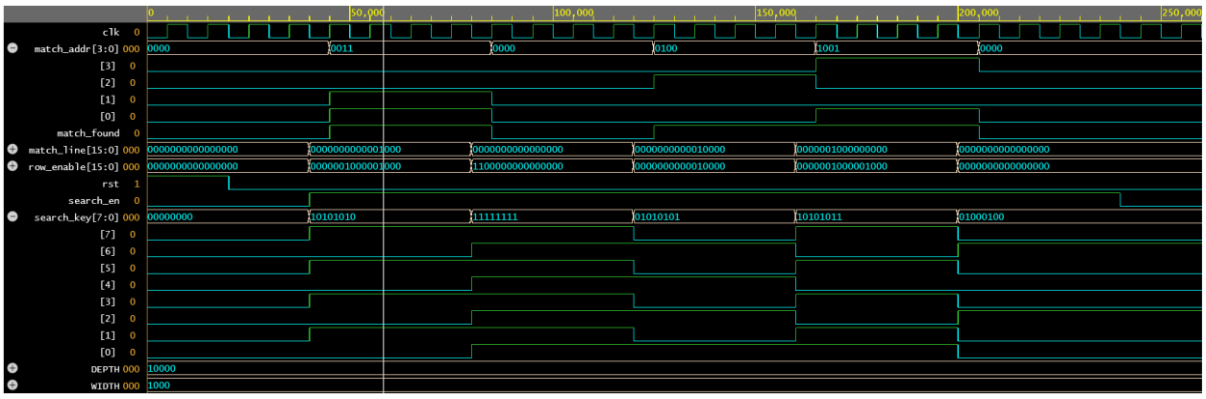


Figure 5. Simulation results of match-line activation waveform, selective waveform, search match and miss waveforms.

The total performance comparison of the Traditional CAM, the previously created LPCAM architecture, and the suggested FPGA-based LPCAM architecture is shown in Table 1. Power consumption, search latency, throughput, energy efficiency, FPGA resource use, and switching activity are among the important performance indicators taken into account in the comparison. Because all match-lines are activated simultaneously during

search operations, the classic CAM architecture has the maximum power usage. By using selective discharge mechanisms and low-power match-line sensing, the previously suggested LPCAM dramatically increases power efficiency, lowering overall power consumption from 11 mW to 6 mW. By further reducing dynamic switching activity through adaptive match-line activation and selective evaluation techniques, the proposed FPGA-based LPCAM builds upon this foundation and lowers overall power consumption to 4.4 mW. Compared to 3 ns for LPCAM and 4 ns for traditional CAM, FPGA-based LPCAM achieves the lowest search latency of 2.6 ns. Consequently, the throughput increases to 385 Msearch/sec, surpassing both previous systems.

Table 1. Performance comparison.

Metric	**Traditional CAM**	**LPCAM**	**Proposed FPGA-Based LPCAM**
Total Power	11.0 mW	6.0 mW	4.4 mW
Search Latency	4 ns	3 ns	2.6 ns
Throughput	250 Msearch/sec	333 Msearch/sec	385 Msearch/sec
Energy/Search	80 pJ	45 pJ	32 pJ
EDP	240 pJ·ns	135 pJ·ns	83 pJ·ns
LUTs	1500	1200	980
Toggle Count	1260	790	520

The proposed LPCAM architecture achieves an Energy Delay Product (EDP) of 83 pJ·ns and requires just 32 pJ per search operation, indicating a significant improvement in energy efficiency. In comparison to both standard CAM and the previous LPCAM implementation, the selective activation technique reduces logic utilization, leading to decreased LUT, Flip-Flop, BRAM, and DSP consumption. Additionally, toggle-count analysis verifies a notable decrease in switching activity, which directly contributes to the dynamic power savings that have been noted.

According to Table 2, FPGA-Based LPCAM achieves the best overall performance in terms of implementation outcomes. By selectively activating candidate match-lines and minimizing unnecessary comparisons, the architecture reduces dynamic power consumption to 98 mW, which is 31.0% less than LPCAM and 47.0% less than Traditional CAM. Energy consumption also decreases to 2.75 pJ/search, a 47.1% improvement over Traditional CAM. Moreover, the reduced search delay is 3.92 ns and the maximum working frequency is 255 MHz due to reduced switching activity. Moreover, the proposed architecture consumes less flip-flops and LUTs and so makes more advantages of FPGA resources. These results suggest that the proposed FPGA-Based LPCAM is well suited for edge-AI, networking and high-throughput search applications as it provides an acceptable trade-off between resource consumption, search performance and power efficiency.

Table 2. Implementation results.

Parameter	**Traditional CAM**	**LPCAM**	**Proposed FPGA-Based LPCAM**
Dynamic Power (mW)	185	142	98
Static Power (mW)	42	41	40
Total Power (mW)	227	183	138
Energy per Search (pJ/search)	5.2	3.95	2.75
Search Delay (ns)	5.6	4.85	3.92
Maximum Frequency (MHz)	178	206	255
Match-Line Activity (%)	100	65	38
Toggle Count per Search	1	0.67	0.39
LUT Utilization	320	278	245
Flip-Flops	192	176	160

Conclusion

The proposed FPGA based LPCAM design utilizes Adaptive Match-Line Activation (AMLA) and Selective Match-Line Evaluation (SMLE) techniques to minimize the unnecessary switching activity and dynamic power consumption as opposed to the traditional CAM architectures that activate all match-lines for every search operation. LUT-based CAM cells are applied to avoid ASIC-specific circuit approaches and optimize the design for FPGA implementation. The proposed LPCAM is implemented and validated on the Xilinx Zynq-7000 (ZC7020) FPGA using the Vivado Design Suite. This architecture drastically reduced the match-line activity and switching transitions, which resulted in lower power consumption and improved energy efficiency, by only activating the candidate match-lines corresponding to the search pattern. The proposed technique achieved 47.0% reduction in dynamic power consumption, 39.2% reduction in total power consumption and 47.1% improvement in energy efficiency per search operation compared to existing CAM and LPCAM implementations. Therefore, the suggested architecture offers a viable and scalable approach to building energy-efficient search engines on contemporary FPGA systems [34]. In future, an AI-driven adaptive match-line prediction system could be added as a part of the proposed FPGA-Based LPCAM.

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